What is claimed is:

1. A nonvolatile semiconductor memory comprising:

a nonvolatile memory cell for storing a charge in response to data; and

a memory cell driving portion for driving the memory cell;

wherein the memory cell driving portion executes a first decision process of deciding pass/fail of the data that is read from the memory cell under a first deciding condition and then applying a signal to the memory cell that is decided as fail to change an amount of charge stored in the memory cell, and a second decision process of deciding the pass/fail of the data that is read from the memory cell under a second deciding condition that is relaxed rather than the first deciding condition.

2. A nonvolatile semiconductor memory according to claim 1, wherein the pass/fail is decided in the first decision process in a write verification by setting a current, which is smaller than a reference current employed in the second decision process, as the reference current, and the pass/fail is decided in the first decision process in an erase verification by setting a current, which is larger than a reference current employed in the second decision process, as the reference current.

3. A nonvolatile semiconductor memory according to claim 1, wherein the pass/fail is decided in the first decision process in a write verification by using a

reference cell whose threshold value is higher than a reference cell employed in the second decision process, and the pass/fail is decided in the first decision process in an erase verification by using a reference cell whose threshold value is lower than a reference cell employed in the second decision process.

4. A nonvolatile semiconductor memory according to claim 1, wherein the memory cell driving portion has a reference current generating circuit for generating a first reference current corresponding to the first deciding condition and a second reference current corresponding to the second deciding condition, and a control portion for driving/controlling the reference current generating circuit.

5. A nonvolatile semiconductor memory according to claim 4, wherein the reference current generating circuit consists of a plurality of transistors whose threshold voltages are different respectively.

6. A nonvolatile semiconductor memory according to claim 4, wherein the reference current generating circuit consists of a reference transistor, a level control transistor connected between a word line and a gate of the reference transistor, and a switching circuit for switching a destination of the reference voltage to any one of the gate of the reference transistor and the level control transistor.

7. A nonvolatile semiconductor memory according to

claim 1, wherein the memory cell is a single gate memory cell that stores the charge in an insulating film in response to the data.

8. A nonvolatile semiconductor memory according to claim 1, wherein the memory cell is a floating gate memory cell that stores the charge in a floating gate in response to the data.

9. A nonvolatile semiconductor memory according to claim 1, wherein the memory cell is a memory cell that corresponds to multiple levels, and the first deciding condition and the second deciding condition are set individually every level.

10. A nonvolatile semiconductor memory operating method of executing data writing or data erasing in a nonvolatile memory cell while verifying a data of the nonvolatile memory cell, comprising:

a first decision process of reading the data from the memory cell under a first deciding condition to decide pass/fail, and applying a signal to the memory cell to change an amount of charge stored in the memory cell if the data is decided as fail; and

a second decision process of reading the data from the memory cell under a second deciding condition, which is relaxed rather than the first deciding condition, to decide the pass/fail;

wherein processes are repeated from the first decision process when the data is decided as fail in the

second decision process.

11. A nonvolatile semiconductor memory operating method comprising:

a first step of setting a start address in an address counter;

a second step of reading a data from a memory cell, which has an address that is set in the address counter, under a first write deciding condition to decide pass/fail;

a third step of applying a write pulse to the memory cell when the data is decided as fail in the second step;

a fourth step of deciding whether or not an address that is set in the address counter is an end address when the data is decided as pass in the second step or when the third step is ended;

a fifth step of changing a value in the address counter when it is decided as no in the fourth step, and then shifting a process to the second step;

a sixth step of setting a start address in the address counter when it is decided as yes in the fourth step;

a seventh step of reading the data from the memory cell, which has the address that is set in the address counter, under a second write deciding condition, which is relaxed rather than the first write deciding condition, to decide pass/fail;

an eighth step of deciding whether or not the address that is set in the address counter is the end address;

a ninth step of changing the value in the address counter when it is decided as no in the eighth step, and then shifting the process to the seventh step; and

a tenth step of being executed when it is decided as yes in the eighth step, and putting the process back in the first step when it is decided as fail in the seventh step.

12. A nonvolatile semiconductor memory operating method according to claim 11, wherein the process goes directly back to the first step when it is decided as fail in the seventh step.

13. A nonvolatile semiconductor memory operating method according to claim 11 or 12, wherein the memory cell is a memory cell that corresponds to multiple levels, and the first deciding condition and the second deciding condition are set individually every level.

14. A nonvolatile semiconductor memory operating method according to claim 11 or 12, wherein the first step to the tenth step are executed in inspection steps, and the first write deciding condition and the second write deciding condition are set by an external inspection equipment.

15. A nonvolatile semiconductor memory operating method comprising:

a first step of setting a start address in an address counter;

a second step of reading a data from a memory cell, which has an address that is set in the address counter,

under a first erase deciding condition to decide pass/fail;

a third step of deciding whether or not an address that is set in the address counter is an end address;

a fourth step of changing a value in the address counter when it is decided as no in the third step, and then shifting a process to the second step;

a fifth step of being executed when it is decided as yes in the third step, and applying an erase pulse collectively to memory cells having the start address through the end address when the memory cell that is decided as fail in the second step is present;

a sixth step of setting the start address in the address counter;

a seventh step of reading the data from the memory cell, which has the address that is set in the address counter, under a second erase deciding condition, which is relaxed rather than the first erase deciding condition, to decide pass/fail;

an eighth step of deciding whether or not the address that is set in the address counter is the end address;

a ninth step of changing the value in the address counter when it is decided as no in the eighth step, and then shifting the process to the seventh step; and

a tenth step of being executed when it is decided as yes in the eighth step, or putting the process back in the first step when the memory cell that is decided as fail in the seventh step is present.

16. A nonvolatile semiconductor memory operating method according to claim 15, wherein the process goes directly to the fifth step when it is decided as fail in the second step, and then an erase pulse is applied collectively to the memory cell having the start address through the end address.

17. A nonvolatile semiconductor memory operating method according to claim 15, wherein the process goes directly back to the first step when it is decided as fail in the seventh step.

18. A nonvolatile semiconductor memory operating method according to any one of claims 15 to 17, wherein the first step to the tenth step are executed in inspection steps, and the first erase deciding condition and the second erase deciding condition are set by an external inspection equipment.